REMARKS

The Office Action of May 13, 2008 has been reviewed in detail and this paper is responsive thereto. Claims 12-28 are pending. Claims 12-19 and 22-26 stand rejected.

Applicant acknowledges that claims 20, 21, 27 and 28 are objected to by the Examiner as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

No new matter has been introduced into the application. As explained in more detail below, Applicants respectfully submit that all remaining pending claims are in condition for allowance.

Other Amendments

Applicant is amending claims 18-19 and 23-26 to replace "sync-control module" with "sync-control circuit." The amendment is supported by the specification as originally filed, *e.g.*, page 23, lines 7-20[1].

Claim Rejections Under 35 USC §103

Claims 12-15, 18 and 22-25 are rejected under 35 USC §103(a) as being unpatentable over US Patent No. 6,445,423 (Bouillet) in view of US Patent No. 6,587,500 (Persson).

Regarding independent claim 12, Bouillet and Persson, either individually or in combination, fail to suggest the feature of "restarting data extraction from the bit stream when the new correlation value exceeds the stored maximum correlation value." The Office Action alleges that Bouillet discloses (Pages 2-3):

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[1] The specification recites, "The symbol timing estimate STE, i.e. the estimated timing of the golden samples is delivered to the sample-and-hold circuit 22 with two signals, i.e. the signal SelSampleNo and the output of counter 33. The free running modulo counter 33, is used as a reference time. The modulo counter 33 is started when the **sync-control circuit** 23 enters the state SYNCFOUND by a start signal Start. The second signal SelSampleNo determines the actual sampling time. When SelSampleNo and modulo counter 33 value are equal the sampling is triggered. When SelSampleNo is incremented by 1 the sample timing is delayed one sample. When SelSampleNo is decremented by 1 sampling takes place one sample earlier. (Page 23, lines 7-20. Emphasis added.)

> restarting data extraction from the bit stream (since the segment sync and timing recovery network 24 is an on-going process, the subsequent digital data will be correlated, compared with the threshold value, and demodulated again.)

However, Bouillet merely discusses a system that receives a continuous data stream for symbol timing recovery in a terrestrial broadcast network. (Column 1, line 56 – column 3, line 36.) In order to provide timing recovery, Bouillet further discusses time equalizer (adaptive equalizer) 34 that first operates in a blind mode. After an elapsed time, the equalizer output is "considered good enough" to assist in timing recovery processes. (Column 5, lines 20-33.[2]) After a further elapsed time, time equalizer 34 operates in a steady-state decision-directed mode. When equalizer operation has stabilized, correlator 320, segment integrator and demodulator 324, segment sync generator 328, and phase detector 310 are reset for segment sync and timing recovery. (Column 4, line 53 – column 5, line 9.[3]) Because timing equalizer 34 operates in a continuous mode (steady-state decision-directed mode), equalizer 34 cannot be restarted while receiving the continuous data stream. Moreover, segment sync and timing recovery network 24 performs timing recovery but does not perform data extraction. According to the teachings of Bouillet, data extraction (corresponding to a bit decision of 0/1) is performed by trellis decoder 40 (as shown in fig. 1), which is further located in the processing chain. (Column 3, lines 4-8.) Persson merely discusses the determination of sampling timing by updating a correlation value threshold and does not remedy the deficiencies of Bouillet. (Column 3, line 59-column 4, line 5.)

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[2] Bouillet recites "When signal acquisition begins, adaptive equalizer 34 operates in a blind mode using a known blind equalization algorithm such as the constant modulus algorithm (CMA), for example. After some time has elapsed, e.g., 50 ms, the equalizer output is considered to be good enough to assist the segment sync and timing recovery processes for developing an appropriate sampling clock from oscillator 336. After symbol timing and the appropriate sampling clock for ADC unit 19 have been established, network 24 continues to receive the equalized output signal from equalizer 34 to improve tracking performance, e.g., in the presence of strong multipath signal conditions. At this time equalizer 34 typically operates in a steady-state decision-directed mode." (Column 5, lines 20-33.)

[3] Bouillet recites "In the preferred embodiment of FIG. 3, initially, when the system is first energized or after the system is reset, VCO 336 is set to operate at a predetermined stable frequency. In this example this frequency corresponds to one of the extreme (maximum or minimum) frequency values within a predetermined frequency range. This initial frequency is significantly offset from the desired symbol timing frequency or a multiple thereof because it has been observed that equalizer 34 converges more rapidly in a blind operating mode by using such an initial frequency rather than an initial frequency that is too close to the desired timing frequency. With the equalizer output being coupled via switch 318 to correlator 320, equalizer 34 is reset and allowed to converge for a predetermined (programmed) amount of time, eg., 50 milliseconds. This interval is chosen to correspond to a time required for the equalizer to exhibit sufficiently stable operation. This interval may be determined empirically in accordance with the requirements of a particular system. At this time, when equalizer operation has stabilized, the phase control network including units 320, 324,328 and 310 is reset and permitted to control the operation of oscillator 336 via filter 334 and control voltage input 349 of oscillator 336. Oscillator 336 begins operation from the initial (reset) predetermined frequency condition mentioned above." (Column 4, line 53-column 5, line 9.)

Independent claim 18 includes the similar feature of "a sync-control circuit configured to receive the correlation value from the packet detector, the sync-control circuit configured to control the data extraction unit for starting or restarting data extraction from the bit stream when the correlation value exceeds a threshold value or a stored maximum correlation value indicating that a data packet has been detected, and configured to store the correlation value that exceeds the threshold value as a maximum correlation value for use as a new threshold value." Also, independent claim 24 includes the feature of "a sync-control circuit configured to receive the correlation value from the packet detector, the sync-control circuit configured to control the data extraction unit for starting or restarting data extraction from the bit stream when the correlation value exceeds a threshold value or a stored maximum correlation value indicating that a data packet has been detected, and configured to store the correlation value that exceeds the threshold value as a maximum correlation value for use as a new threshold value." Claims 13-15, 22-23, and 25 ultimately depend from claims 12, 18, and 24 and are thus patentable for at least the above reasons. Applicant requests reconsideration of claims 12-15, 18, and 22-25.

Moreover, claim 15, which depends from claim 12, also includes the feature of "wherein data extracted prior to restarting data extraction is rejected." The Office Action alleges that (Page 4.):

> Regarding claim 15, Persson et al. disclose wherein data extracted prior to restarting data extraction is rejected (since Persson teaches updating threshold value to reduce the probability of false alarm (Col 3, L21-25), it is obvious that the data extracted from the previous threshold (i.e, false alarm) should be rejected so as to improve quality (official notice is taken here)).

Persson merely discusses the determination of optimum sampling timing (sampling phase) from a set of trigger output values (corresponding to a trigger output state X_k). (Column 3, line 59-column 4, line 5.) The trigger output values are determined from correlation values of each sampling stream with a predetermined bit sequence. The correlation values are fed into a threshold comparator that compares the correlation values with a variable threshold value to generate the trigger output values. The variable threshold is updated to the current correlation value s_k if the current correlation value exceeds the current threshold. (Column 4, lines 32-52.) Persson further discloses a table of phase decision rules 90 in Fig. 5, in which a phase decision is determined based on the trigger output state X_k. (Column 5, lines 9-31.) Persson fails to suggest the rejection of any extracted data. The Office Action alleges that extracted data should be

rejected from the previous threshold if the threshold value is updated in order to reduce the probability of a false alarm. However, the proposed modification to Persson would alter the intended purpose, in which trigger output states (corresponding to extracted data in the proposed modification) would be rejected when the threshold changes. Consequently, the proposed modification would disrupt the phase decision process as taught by Persson.

Claims 16, 17, 19, and 26 are rejected under 35 USC §103(a) as being unpatentable over Bouillet in view of Persson and in further view of US Patent No. 5,619,542 (Gurney).

Claims 16, 17, 19, and 26 ultimately depend from claims 12, 18, and 26. Moreover, Gurney merely describes methods and devices for predicting a symbol timing estimation in a digital radio receiver and fails to remedy the deficiencies of Bouillet and Persson. (Column 1, lines 42-44.) Applicant thus requests reconsideration of claims 16, 17, 19, and 26.

Moreover, claim 17 includes the additional feature of "wherein timing of the sampling of bits is **continuously** tracked by comparing timing of symbols within an oversampled bitstream with actual timing of the sampling of bits and correcting the timing of the sampling of bits if a deviation between the timing of the sampling of bits and the timing of the symbols exceeds a value." (Emphasis added.) The Office Action alleges that (Page 7):

> Regarding claim 17, Bouillet et al and Persson disclose all the subject matters above except for the specific teaching of timing of sampling is continuously tracked by comparing timing of symbols within an oversampled bit stream with actual timing of the sampling and correcting the timing of the sample if a deviation between the timing of the sampling and the timing of the symbols exceeds a value.
>
> Gurney et al, in the same field of endeavor, disclose an optimal sampling and timing estimation system, where oversampled data and optimal sampling phase are coupled with symbol timing decimator (as shown in Fig. 2). This provides highest possible signal to noise ratio in a digital receiver. Therefore, it is obvious to one of ordinary skill in art at to combine the efficient timing estimation system of Gurney et al with the digital receiver of Bouillet et al. By doing so, provide optimal receiver system with better reception signal quality, lessen power consumption, and reduce production cost.

However, Gurney merely discusses timing of a received signal prior to processing bits for a desired time slot, and consequently the timing of the sampling of bits cannot be continuously tracked. (Column 3, lines 2-10.[4])

Applicants therefore respectfully request reconsideration of the pending claims and a finding of their allowability. A notice to this effect is respectfully requested. Please feel free to contact the undersigned should any questions arise with respect to this case that may be addressed by telephone.

Respectfully submitted,

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By: Kenneth F. Smolik

Kenneth F. Smolik
Registration No. 44,344
BANNER & WITCOFF, LTD.
10 South Wacker Drive, Suite 3000
Chicago, IL 60606
Telephone: 312-463-5000
Facsimile: 312-463-5001

4 Gurney recites "By allowing the symbol timing estimator (204) to **run prior** to the desired reception or time slot, storing the calculated symbol timing estimate value in a storage register, and **later applying** the predicted symbol timing estimate to the desired digital received data, the entire RAM slot buffer described above can be eliminated. Since the radio channel is slowly changing, **the prior symbol timing estimate value is equally valid for the desired time slot.**" (Column 3, lines 2-10. Emphasis added.)